CLAIMS

1. A nonvolatile semiconductor memory comprising:

a memory cell array having a memory cell unit formed from only one memory cell and two select gate transistors sandwiching the memory cell;

a bit line connected to an associated one of the select gate transistors;

a sense amplifier connected to the bit line; and

a control circuit which controls a programming operation for the memory cell, wherein the programming operation is executed only one time, a threshold voltage of the memory cell is higher than a read voltage, and the highest limit of the threshold voltage of the memory cell is infinite.

2. The nonvolatile semiconductor memory according to claim 1, wherein the programming operation is executed by using a program voltage sufficient to complete programming of the memory cell.

3. The nonvolatile semiconductor memory according to claim 1, wherein a program verify operation is executed after the programming operation and detects whether the threshold voltage of the memory cell is higher than the read voltage.

4. The nonvolatile semiconductor memory according to claim 1, wherein a program verify operation is inhibited after the programming operation.

5. The nonvolatile semiconductor memory according to claim 1, wherein the memory cell has a control gate electrode and a floating gate electrode.

6. The nonvolatile semiconductor memory according to claim 1, wherein the programming operation is executed by using an F-N tunneling phenomenon.

7. The nonvolatile semiconductor memory according to claim 1, wherein the sense amplifier has a latch function.

8. A nonvolatile semiconductor memory comprising:

a memory cell array having a memory cell unit formed from only one memory cell and two select gate transistors sandwiching the memory cell;

a bit line connected to an associated one of the select gate transistors;

a sense amplifier connected to the bit line; and

a control circuit which controls an erasing operation for the memory cell, wherein the erasing operation is executed only one time, a threshold voltage of the memory cell is lower than a read voltage, and the lowest limit of the threshold voltage of the memory cell is infinite.

9. The nonvolatile semiconductor memory according to claim 8, wherein the erasing operation is executed by using an erase voltage sufficient to complete erasing of the memory cell.

10. The nonvolatile semiconductor memory according to claim 8, wherein an erase verify operation is executed after the erasing operation and detects whether the threshold voltage of the memory cell is lower than the read voltage.

11. The nonvolatile semiconductor memory according to claim 8, wherein an erase verify operation is inhibited after the erasing operation.

12. The nonvolatile semiconductor memory according to claim 8, wherein the memory cell has a control gate electrode and a floating gate electrode.

13. The nonvolatile semiconductor memory according to claim 8, wherein the erasing operation is executed by using an F-N tunneling phenomenon.

14. The nonvolatile semiconductor memory according to claim 8, wherein the sense amplifier has a latch function.